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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/711,066	08/20/2004	Chih-Chiang Wen	MTKP0164USA	5065

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EXAMINER	
PICH, PONNOREAY	
ART UNIT	**PAPER NUMBER**
2135	

NOTIFICATION DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/711,066	WEN ET AL.	
	Examiner	Art Unit	
	PONNOREAY PICH	2135	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 June 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 June 2008* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claims 1-17 are pending. It is noted that applicant did not submit any set of claims with the arguments submitted on 6/30/08. Therefore it is assumed that applicant did not make any amendments to the claims and all arguments are directed towards to original set of claims.

Drawings

The replacement drawings were received on 6/30/08. These drawings are acceptable.

Response to Arguments

Applicant's arguments filed 6/30/08 have been fully considered but they are not persuasive.

Applicant disagreed with the rejection of claim 1 under 35 USC 103 stating that Ishikawa teaches using a microprocessor to drive a memory controller to directly access stored data and applicant's claim 1 is distinguished in that the present invention skips the step of using a direct memory controller and Ishikawa accesses a disk and does not involve encrypted data. This argument was not persuasive. Claim 1 was rejected as obvious over the teachings of applicant's admitted prior art (AAPA) in view of Ishikawa. One cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.,* 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). Applicant's argument focuses only on Ishikawa and fails to address how claim 1 distinguishes from the combined teachings of AAPA and Ishikawa and as such,

also fails to comply with 37 CFR 1.111(b) since it fails to address the rejection made in the last Office action.

With respect to claim 2, applicant argues that claim 2 discloses using a register module to store an encrypted instruction which is not the same as the cache in Ishikawa and that in applicant's disclosure, the encrypted data can be immediately transmitted to the decryption module to immediately generate the corresponding decryption instruction. Again, applicant's argument was not persuasive. Claim 2 was rejected as obvious over the teachings of applicant's admitted prior art (AAPA) in view of Ishikawa. One cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.,* 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). Applicant's argument focuses only on Ishikawa and fails to address how claim 2 distinguishes from the combined teachings of AAPA and Ishikawa and as such also fails to comply with 37 CFR 1.111(b) since it fails to address the rejection made in the last Office action. Further, what is disclosed in applicant's disclosure but not claimed is irrelevant because although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993). What applicant discussed for the argument of claim 2 is disclosed in the specification was not claimed.

As per claim 5, applicant disagreed with the examiner that the further limitation recited therein would have been obvious to one skilled in the art and stated that the rejection relied on mere conclusory statements. The examiner respectfully disagrees.

The examiner explained in the rejection of claim 5, why the invention claimed therein would have been obvious based on the teachings of AAPA and Ishikawa--this is not mere conclusory statements as applicant is alleging. Applicant has failed to comply with 37 CFR 1.111(b) since applicant has failed to point out where the examiner's reasoning as set forth in the rejection of claim 5 contains any errors instead labeling the reasoning set forth by the examiner as mere conclusory statements.

With respect to claim 6, applicant asserts that locating the storage apparatus in a chip is not the same as Ishikawa because the storage apparatus includes the encrypted data. Again, applicant's argument was not persuasive. Claim 6 was rejected as obvious over the teachings of applicant's admitted prior art (AAPA) in view of Ishikawa. One cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.,* 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). Applicant's argument focuses only on Ishikawa and fails to address how claim 6 distinguishes from the combined teachings of AAPA and Ishikawa and as such also fails to comply with 37 CFR 1.111(b) since it fails to address the rejection made in the last Office action.

As per claim 7, applicant states that the microprocessor in AAPA is not connected to the decryption module, but is instead connected to the storage apparatus. The examiner respectfully notes that the language of claim 7 requires that the microprocessor is electronically connected to the decryption module. Figure 1 of AAPA

showing the microprocessor 28 being electronically connected to decryption module 24 via storage apparatus 2 meets the requirements of the claimed language.

With respect to claim 7 applicant states that the examiner used Ishikawa to show utilizing a processor to drive the instruction access controller to control a storage apparatus to transmit data for access, then disagreed that Ishikawa showed this. Applicant states that Ishikawa shows data transfer between a microprocessor and a disk using an interface control unit and a cache. The examiner respectfully disagrees. The portion of Ishikawa cited by the examiner (col 1, lines 25-29 and col 5, lines 23-29) clearly shows that the data transfer control unit 40 of Ishikawa is used to control transfer of data to and from a storage apparatus. Further, the data transfer control unit itself is driven/controlled by the microprocessor 3 setting registers 401 and 501 of the data transfer control unit 40. The data transfer control unit 40 can be considered an instruction access controller which controls a storage apparatus to transmit data for access.

Claims 3 and 10 were argued as allowable due to dependency on claims 1 and 7. However, because claims 1 and 7 are not allowable, neither are claims 3 and 10.

As per claims 4 and 11, applicant argues that encrypting the address where the encrypted instructions are located and then storing a key that has to be read to decrypt the address is far from obvious. Applicant points out that Lee encrypts the address but doesn't use a stored key while Kawaguchi uses a stored key but doesn't encrypt the address. The examiner respectfully disagrees. Again applicant has performed a piece-meal analysis of the references rather than considering what the references as a whole

would have made obvious to one of ordinary skill in the art. Neither reference by themselves would make obvious the limitations further recited in claims 4 and 11, but if one were to consider the teachings of both Lee and Kawaguchi as a whole, it would have been obvious. Applicant sates that the examiner has not provided a sufficient reason or analysis of why the disclosures of the references should be combined. The examiner respectfully disagreed. The last paragraph on page 11 of the last office action provides an analysis and reason of why the disclosure of the references should be combined. Applicant merely stating that the examiner did not provide sufficient reason and analysis when the examiner clearly did does not comply with 37 CFR 1.111(b).

With respect to claim 8, applicant argues that the firmware update disclosed in Hu is the same as claim 8 of the present application because nothing in Hu is encrypted. This argument is also traversed because whereas the rejection of claim 8 is based on an analysis of what would have been obvious based on the combined teachings of AAPA, Ishikawa, and Hu, applicant only focuses on Hu. One cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.,* 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

With respect to claim 13 applicant disagreed that it would have been obvious to a person skilled in the art to use non-volatile memory as the storage apparatus. This argument fails to comply with 1.111(b) because it fails to specifically point out the supposed error in the rejection. Applicant may disagree with the examiner's reasoning, but need to provide proof and rationale for why applicant's position is correct.

Applicant's arguments with respect to claim 13 amounts to mere allegation of patentability.

Any remaining arguments not specifically addressed were directed towards allowance of the claims due to the claims being allowable due to dependency on an allowable claim. However, as no claims are allowable, the dependency arguments are traversed.

The prior rejections are repeated below for record.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The examiner submits that a person of ordinary skill in the art at the time applicant's invention was made is someone having at least a BS in Electrical/Computer Engineering (or someone with equivalent industry experience).

Claims 1-2, 5-7, 12, and 14-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over applicant's admitted prior art (herein referred to as AAPA) in view of Ishikawa (EP 0440243A2).

Claim 1:

AAPA discloses that the following was well known in the prior art:

1. Decrypting encrypted instruction to generate a decrypted instruction (paragraphs 4-5).
2. Utilizing the microprocessor to operate according to the decrypted instruction (paragraphs 4-5).

AAPA does not disclose the following limitations were known in the prior art:

1. Utilizing an instruction access controller (IAC) to access the encrypted instruction.
2. Utilizing a microprocessor to drive the instruction access controller to access the encrypted instruction.

However, Ishikawa discloses utilizing an IAC to access stored data (col 1, lines 15-18 and 25-29; col 5, lines 8-14; and col 7, lines 33-47). Ishikawa discloses utilizing a microprocessor to drive the instruction access controller to access the stored data (col 1, lines 25-29 and col 5, lines 23-29 and 50-55). Recall that the encrypted instruction disclosed by AAPA is nothing more than data stored in an external memory (Fig 1 and paragraphs 4-5).

At the time applicant's invention was made, it would have been obvious to one of ordinary skill in the art to modify the chip 12 disclosed by AAPA such that rather than use a DMA controller 20 and memory controller 22 to access encrypted instructions stored in external memory 14, an IAC (i.e. memory controller) that is driven by a processor as disclosed by Ishikawa was utilized instead. It would have been obvious to

one skilled in the art to do so because modifying AAPA's chip in the manner discussed is nothing more than the simple substitution of one known element for another to obtain predictable results. In this case the predictable result is accessing stored encrypted instruction by use of a memory controller/IAC that is driven by a processor instead of one driven by a DMA controller.

Claim 2:

The limitation further recited in claim 2 is obvious to the combination invention of AAPA and Ishikawa. Ishikawa discloses providing a register module (col 1, lines 41-44 and col 7, lines 33-36 and 44-47: *i.e. the controller's cache*); and driving the register module to store the data accessed by the instruction access controller according to an address provided by the instruction access controller (col 7, lines 20-24, 33-36, and 44-47). The instruction being encrypted instruction is obvious to the combination invention because AAPA discloses the data being encrypted instruction (paragraphs 4-5).

Claim 5:

AAPA and Ishikawa teachings make obvious to limitations further recited in claim 5. Note that the DMA controller and memory controller disclosed by AAPA is located in a chip along with the microprocessor (Fig 1). The proposed modification of AAPA's chip in light of Ishikawa's teachings as discussed in claim 1 involves merely replacing the DMA controller and memory controller taught by AAPA with an IAC as taught by Ishikawa. Since the DMA controller and memory controller performs a similar function as the IAC taught by Ishikawa, then it would have been obvious to one skilled in the art when replacing the DMA controller and memory controller of AAPA to still keep the

component which controls memory access within the chip along with the microprocessor. As such, based on AAPA and Ishikawa's teachings it would have been obvious to one skilled in the art to locate the instruction access controller and the microprocessor in a chip.

Further, AAPA discloses wherein the encrypted instruction is stored in a storage apparatus connected to the chip (Fig 1, external memory 14 and paragraphs 4-5).

Claim 6:

AAPA and Ishikawa teachings make obvious to limitations further recited in claim 6. AAPA discloses wherein the encrypted instruction is stored in a storage apparatus (Fig 1, external memory 14 and paragraphs 4-5). As per the limitation of locating the storage apparatus, the instruction access controller, and the microprocessor in a chip, note that it is obvious to locate the instruction access controller and microprocessor in a chip for the same reasons discussed in claim 5. As per locating the storage apparatus which contains the encrypted instructions in the chip also, note that in Ishikawa's invention, when data is read from an external storage, the data is also cached in an internal cache in the chip (col 5, lines 7-14; col 6, lines 26-35; and col 7, lines 33-47). As such, in light of Ishikawa's teachings, it would have been obvious to one skilled in the art to also locate the storage apparatus containing the encrypted instruction in the chip along with the instruction access controller and the microprocessor. One skilled would have done so because caching encrypted instruction in cache memory on a chip would allow for quicker read of the encrypted instruction by the processor.

Claim 7:

AAPA discloses:

1. A storage apparatus for storing an encrypted instruction (Fig 1, external memory 14 and paragraphs 4-5).
2. An instruction access controller (IAC) electronically connected to the storage apparatus for accessing the encrypted instructions from the storage apparatus (Fig 1, memory controller 22 and paragraphs 4-5).
3. A decryption module electronically connected to the storage apparatus for decrypting the encrypted instruction to generate a decrypted instruction (Fig 1, decryption module 24 and paragraphs 4-5).
4. A microprocessor electronically connected to the instruction access controller and the decryption module, the microprocessor receiving the decrypted instruction from the decryption module to operate (Fig 1, microprocessor 28 and paragraphs 4-5).

AAPA does not disclose the microprocessor is for driving the instruction access controller to control the storage apparatus to transmit the encrypted instructions to the decryption module. Note that in AAPA's prior art invention, the DMA controller 20 instead does this driving. However, Ishikawa discloses utilizing an IAC to access stored data (col 1, lines 15-18 and 25-29; col 5, lines 8-14; and col 7, lines 33-47). Ishikawa discloses utilizing a microprocessor to drive the instruction access controller to control a storage apparatus to transmit data for access (col 1, lines 25-29 and col 5, lines 23-29

and 50-55). Recall that the encrypted instruction disclosed by AAPA is nothing more than data stored in an external memory (Fig 1 and paragraphs 4-5).

In light of Ishikawa's teachings it would have been obvious to one skilled in the art to modify the prior art invention disclosed by AAPA such that rather than have the DMA controller drive the IAC to control the storage apparatus to transmit the encrypted instruction to the decryption module, the processor is instead utilized for said purpose. It would have been obvious to one skilled in the art to do so because modifying AAPA's chip in the manner discussed is nothing more than the simple substitution of one known element for another to obtain predictable results. In this case the predictable result is accessing stored encrypted instruction by use of a memory controller/IAC that is driven by a processor instead of one driven by a DMA controller.

Claim 12:

Ishikawa further discloses wherein the instruction access controller, the decryption module, and the microprocessor are located in a chip, and the storage apparatus is connected to the chip (Fig 1).

Claims 14 and 17:

AAPA further discloses wherein the chip is a controlling chip of a disc player, and the decrypted instruction is a firmware of the disc player (paragraphs 4-5).

Claim 15:

Much of the limitations further recited in claim 15 are similar to what is recited in claim 6 and those limitations are rejected for similar reasons as discussed in claim 6. The difference is that claim 15 additionally recite that the decryption module is also

located in the chip. However, note that AAPA also discloses that the decryption module is located in the chip (Fig 1).

Claim 16:

AAPA further discloses wherein the storage apparatus is a volatile memory (paragraph 6, *i.e. SRAM*).

Claims 3 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over applicant's admitted prior art (herein referred to as AAPA) in view of Ishikawa (EP 0440243A2) in further view of Kawaguchi (US 7,228,436).

Claim 3:

AAPA and Ishikawa do not explicitly disclose providing a key storage unit for storing a key; wherein the step of decrypting the encrypted instruction further comprises reading the key to decrypt the encrypted instruction.

However, AAPA's chip decrypts the encrypted instruction (paragraphs 4-5). Further, Kawaguchi discloses an integrated circuit wherein encrypted instructions are read in and decrypted (col 7, lines 32-48). Kawaguchi discloses providing a key storage unit for storing a key (Fig 1, register 107); wherein the step of decrypting the encrypted instruction further comprises reading the key to decrypt the encrypted instruction (col 8, lines 3-6).

At the time applicant's invention was made, it would have been obvious to further modify AAPA and Ishikawa's combination invention such that the chip is provided with a

key storage unit for storing a key; wherein the step of decrypting the encrypted instruction further comprises reading the key to decrypt the encrypted instruction. It would have been obvious to one skilled in the art to modify AAPA and Ishikawa's combination invention in the manner discussed because while AAPA discusses decrypting the encrypted instruction, AAPA is silent with respect to exactly how the decryption is done. Incorporating Kawaguchi's teachings so that the decryption is done using a stored decryption key in the manner discussed is nothing more than applying a known technique to a known device ready for improvement to yield predictable results.

Claim 10:

Claim 10 further recites limitations substantially similar to what is recited in claim 3 and is rejected for similar reasons. Claim 10 refers to an apparatus used to implement the method of claim 3.

Claims 4 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over applicant's admitted prior art (herein referred to as AAPA) in view of Ishikawa (EP 0440243A2) in further view of Lee (US 2004/0177262) and Kawaguchi (US 7,228,436).

Claim 4:

AAPA and Ishikawa do not explicitly disclose providing a key storage unit for storing a key; wherein the step of accessing the encrypted instruction further comprises reading the key to decrypt the access address of the encrypted instruction.

However, Lee discloses of a data protection method wherein the address of data is stored in encrypted form and to access the data, the address of the data has to be decrypted (paragraphs 30 and 42). Further, Kawaguchi discloses encryption/decryption via use of a stored key, whereby a key storage unit is provided for storing a key and the encrypted data is accessed by reading the key to decrypt the encrypted data (col 7, lines 32-48 and Fig 1, register 107).

At the time applicant's invention was made, it would have been obvious in light of Lee and Kawaguchi's teachings to modify AAPA and Ishikawa's combination invention such that the stored instruction disclosed by AAPA was further protected by encrypting the address of where the encrypted instructions were located and to access the encrypted instructions, a key stored in a key storage unit has to be read to decrypt the access address of the encrypted instruction. It would have been obvious to one skilled in the art to modify AAPA and Ishikawa's combination invention in the manner discussed because incorporating Lee and Kawaguchi's teachings as discussed is use of known techniques to improve similar devices in the same way.

Claim 11:

Claim 11 further recites limitations substantially similar to what is recited in claim 4 and is rejected for similar reasons. Claim 11 refers to an apparatus used to implement the method of claim 4.

Claims 8-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over applicant's admitted prior art (herein referred to as AAPA) in view of Ishikawa (EP 0440243A2) in further view of Hu (US 6,170,043).

Claim 8:

AAPA and Ishikawa discloses a register module (i.e. cache) electronically connected to the instruction access controller (Ishikawa: col 1, lines 41-44 and col 7, lines 33-36 and 44-47), the storage apparatus and the decryption module for storing the encrypted instruction (AAPA: paragraphs 4-5) and transmitting the encrypted instruction to the decryption module (AAPA: paragraphs 4-5).

AAPA and Ishikawa do not explicitly disclose the storing is according to an address provided by the instruction access controller. However, note that the encrypted instructions disclosed by AAPA are encrypted firmware (paragraphs 2-4). Hu further discloses updating firmware (col 4, lines 20-29). When firmware is updated, the new firmware instructions are stored in a storage apparatus according to an address provided by an instruction access controller that is driven by a processor (col 3, lines 29-36; col 5, lines 14-18; and col 6, lines 17-28).

At the time applicant's invention was made, it would have been obvious to modify AAPA and Ishikawa's combination invention according to the limitations recited in claim 8 in light of Hu's teachings by allowing firmware to be updated and stored according to an address provided by the instruction access controller. It would have been obvious to one skilled in the art to do so because incorporating Hu's teachings in the manner

discussed is applying a known technique to a known device ready for improvement to yield predictable results.

Claim 9:

Ishikawa further discloses wherein the register module functions as a cache memory (col 1, lines 41-44 and col 7, lines 33-36 and 44-47).

Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over applicant's admitted prior art (herein referred to as AAPA) in view of Ishikawa (EP 0440243A2) in further view of Takahashi et al (US 5,825,878).

Claim 13:

AAPA and Ishikawa does not explicitly disclose where the storage apparatus is a non-volatile memory. Note that AAPA discloses the storage apparatus is SRAM (paragraph 6). However, Takahashi discloses that non-volatile memory could be used in place of SRAM for storage of data (col 2, lines 54-56). At the time applicant's invention was made, it would have been obvious to one skilled in the art to utilize a non-volatile memory as the storage apparatus in AAPA and Ishikawa's combination invention. It would have been obvious to do so because use of non-volatile memory in place of SRAM is simple substitution of one known element for another to obtain predictable results.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to PONNOREAY PICH whose telephone number is (571)272-7962. The examiner can normally be reached on 9:00am-4:30pm Mon-Thurs.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kim Vu can be reached on 571-272-3859. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Ponnoreay Pich/
Examiner, Art Unit 2135
/KimYen Vu/
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